

ADVANCED EYE ANALYSIS FOR MIPI D-PHY

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ROHDE & SCHWARZ

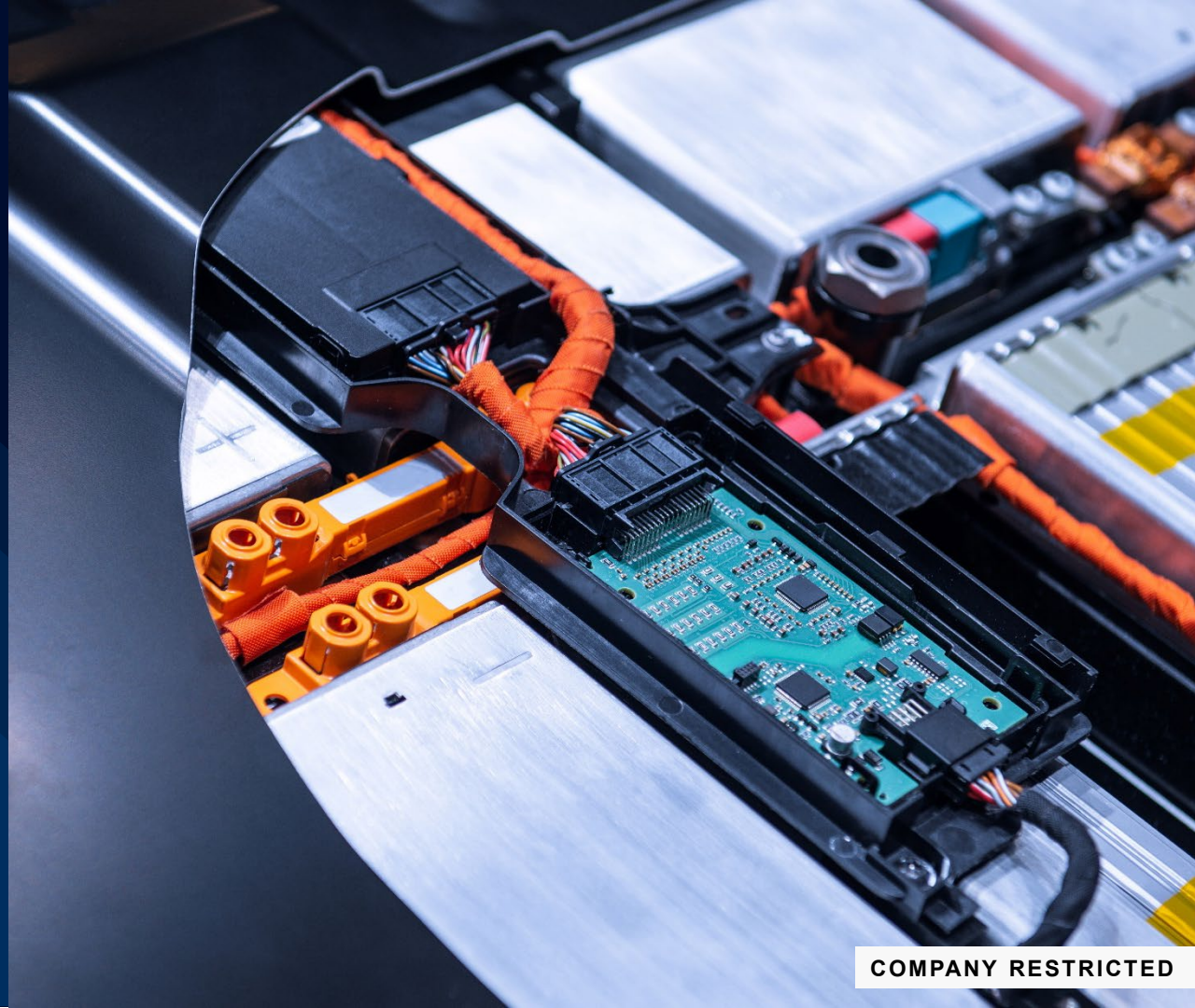
Make ideas real



COMPANY RESTRICTED

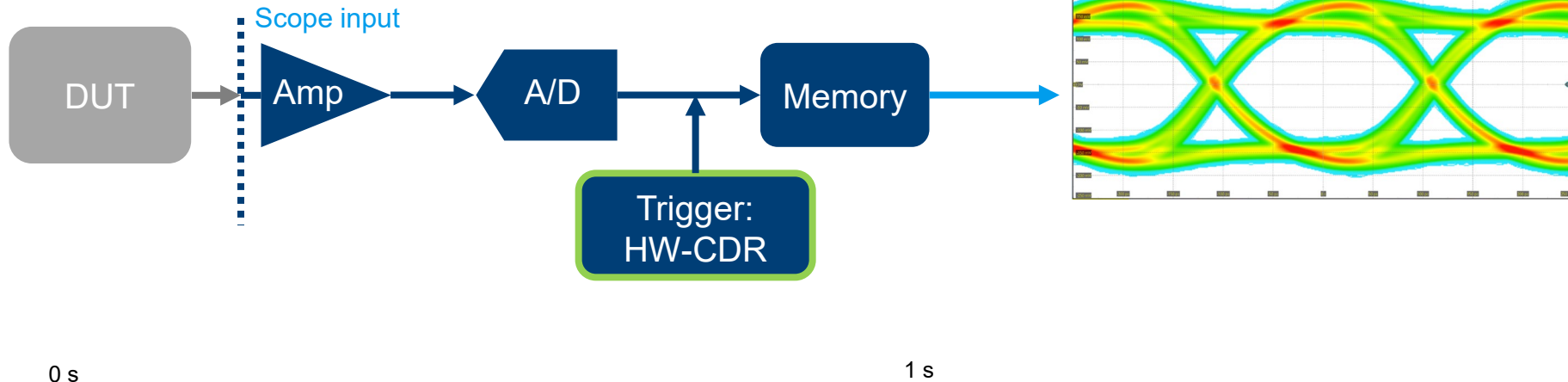
CONTENT

1. CDR Trigger
2. Advanced Eye Analysis
3. How to debug
4. Q&A



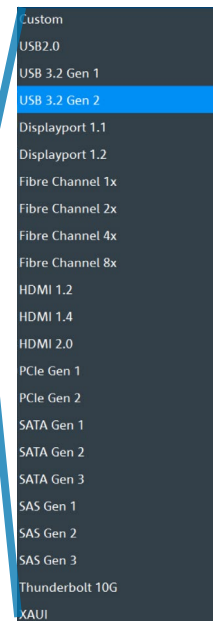
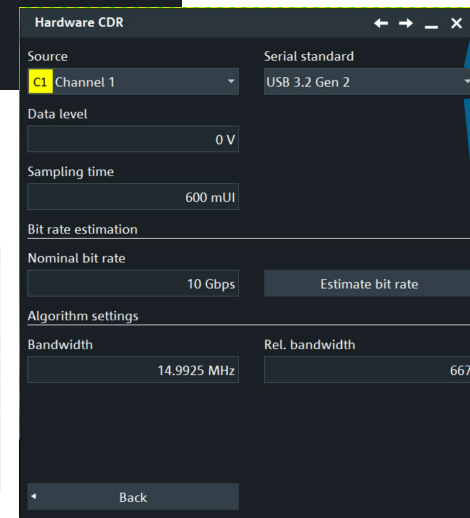
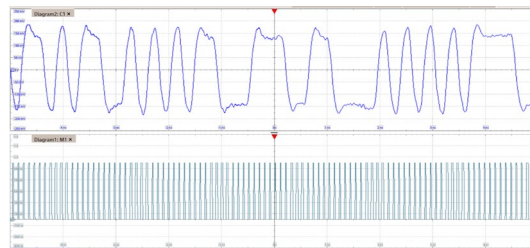
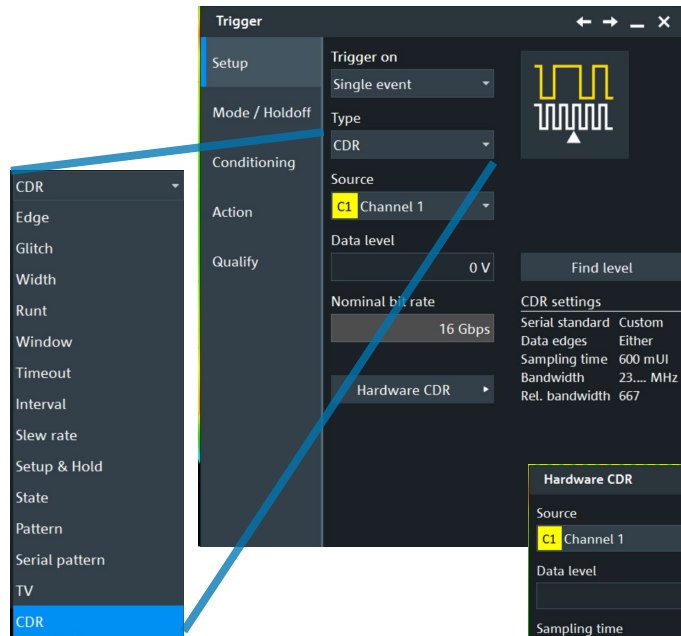
HW-BASED CLOCK-DATA-RECOVERY TRIGGER

- ▶ Eye Analysis based on Hardware implemented Clock-Data-Recovery (CDR)
 - CDR is part of the Trigger circuitry
 - CDR locks once and runs continuously
 - CDR is applicable for both Eye approaches: Bit sequence and Individual bits („Live Eye“)



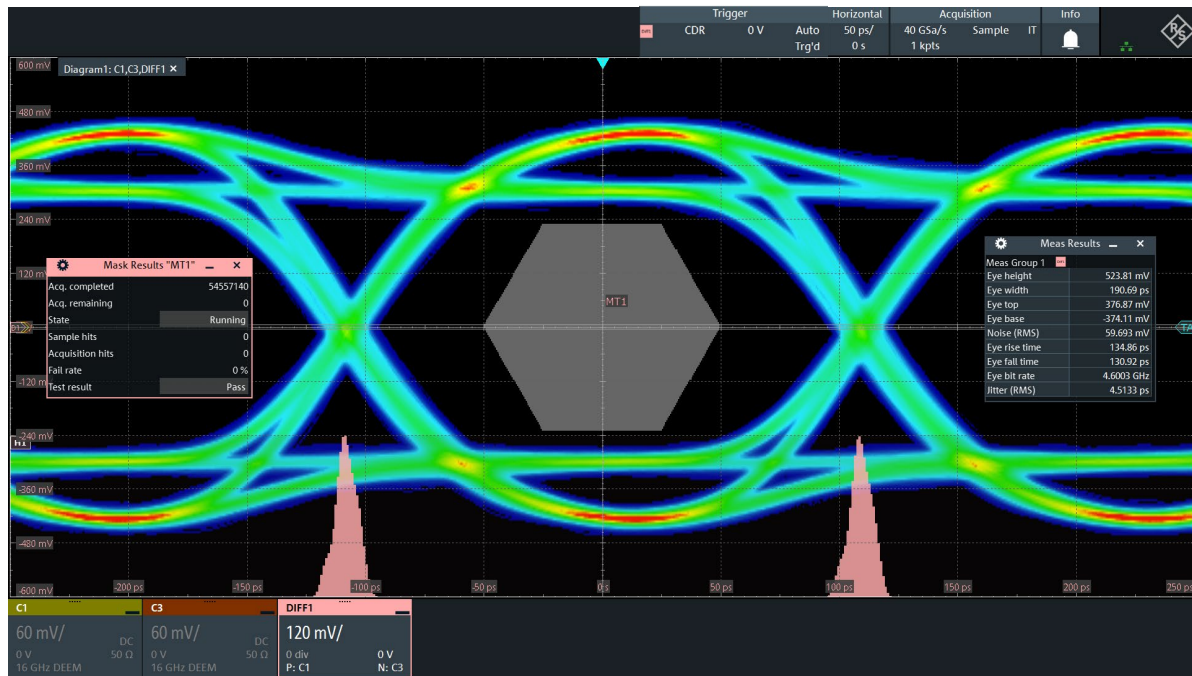
DETAILS OF CDR TRIGGER

- ▶ Source:
 - any analog channels
- ▶ Combinable with:
 - differential signal math and real-time deembedding
- ▶ Nominal bit rate:
 - 21 kbps to 16 Gbps
- ▶ Configurable BW:
 - 1/500 to 1/3000 of nominal bit rate
- ▶ CDR timing can be saved as math waveform



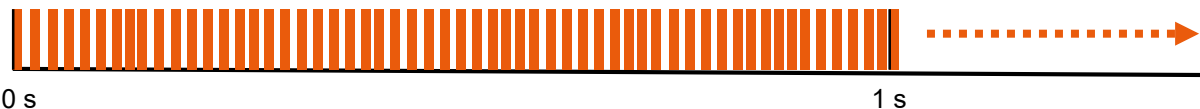
HW-CDR TRIGGER FOR "LIVE EYE"

- ▶ Options: RTP-K136/137
- ▶ HW-CDR up to 8/16 Gbps
 - Trigger individual bits based on embedded clock
- ▶ Benefits
 - Fast results due to high acquisition rate (>400,000 max)
 - Continuously CDR running as time reference
 - Combinable with HW implemented Histogram and Mask Test
 - Combinable with Realtime Deembedding



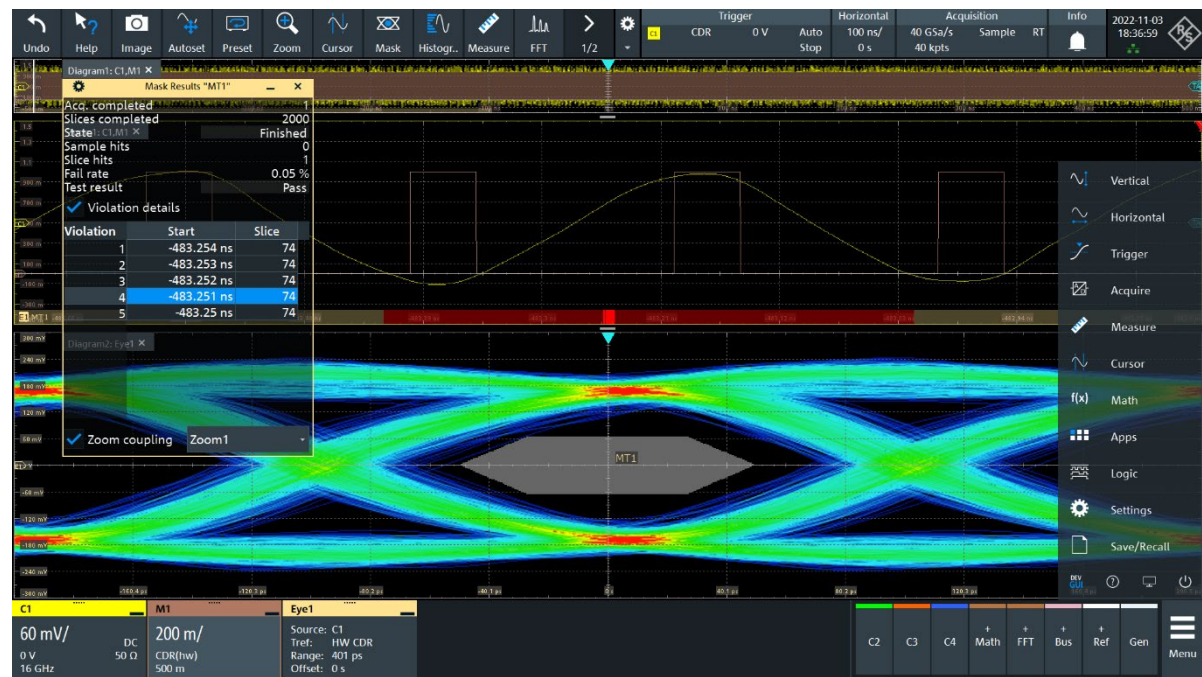
Signal-integrity debugging:

- Fast glance on Jitter / Noise
- Long-term monitoring
- Use Mask and Histogram



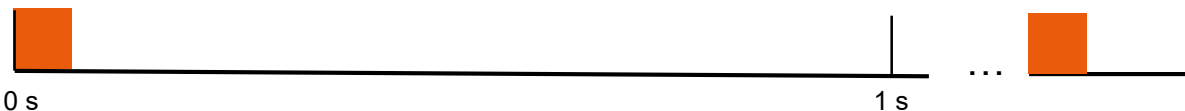
HW-CDR TRIGGER FOR ADVANCED EYE ANALYSIS

- ▶ Options: RTP-K136/137
- ▶ HW-CDR up to 8/16 Gbps
 - Bit folding based on continuously running HW-CDR
- ▶ Powerful capabilities
 - HW-CDR as Math available
 - Powerful Filter & Qualify options
 - Saving of Data Eye
 - Automated eye measurements
 - Mask test w/ EyeStripe function
 - Mask test library for typical interface standards



Signal-integrity characterization:

- Based on a long bit sequence
- Transmitter output and signal path characteristic
- Use Mask and Histogram

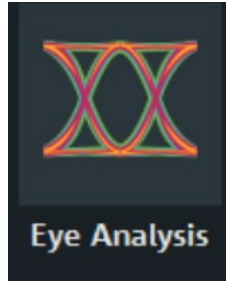


ADVANCED EYE ANALYSIS

EASY SETUP IN 3 STEPS

Quick start with Eye Analysis

1. Select Source
2. Hardware CDR: Select Serial Standard
3. Set State: On



The screenshot displays the 'Eye Analysis' software interface. The 'Setup' tab is active, showing the 'Eye 1' configuration. The 'State' is set to 'Off' (labeled '3.'). The 'Source' is set to 'C1W1' (labeled '1.'). The 'Hardware CDR' is selected. The 'Serial standard' is set to 'USB 3.2 Gen 2' (labeled '2.'). The 'Nominal bit rate' is 10 Gbps, and the 'Bandwidth' is 14.9925 MHz. The 'Rel. bandwidth' is 667. The 'Sampling time' is 600 mUI. The 'Unit interval (UI)' is 2. The 'Position UI' is 0 UI. The 'Back' button is visible at the bottom left of the Hardware CDR settings panel.

ADVANCED EYE ANALYSIS

TUNE YOUR SETUP

Advanced settings:

► Display:

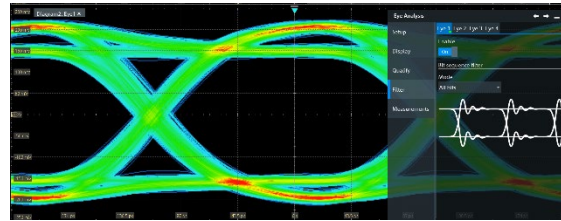
- color table, persistence,
- „Eye stripe“
- Slices per acq. (default 2000, max. 2.5 M)

► Qualify:

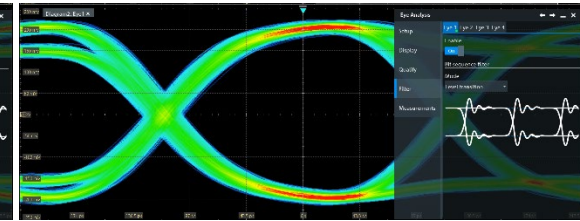
- Gate
- Signal

► Filter:

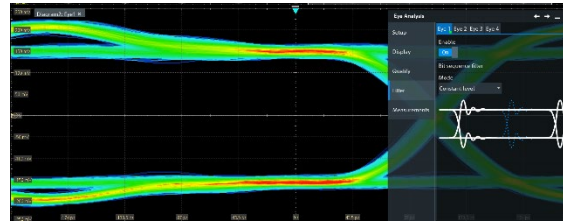
- All bits / level transition / constant level
- Bit pattern



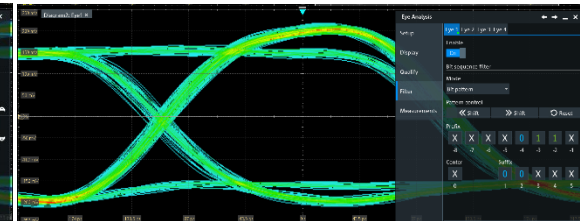
All bits



Level transition



Constant level



Bit pattern

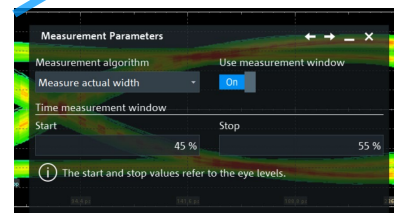
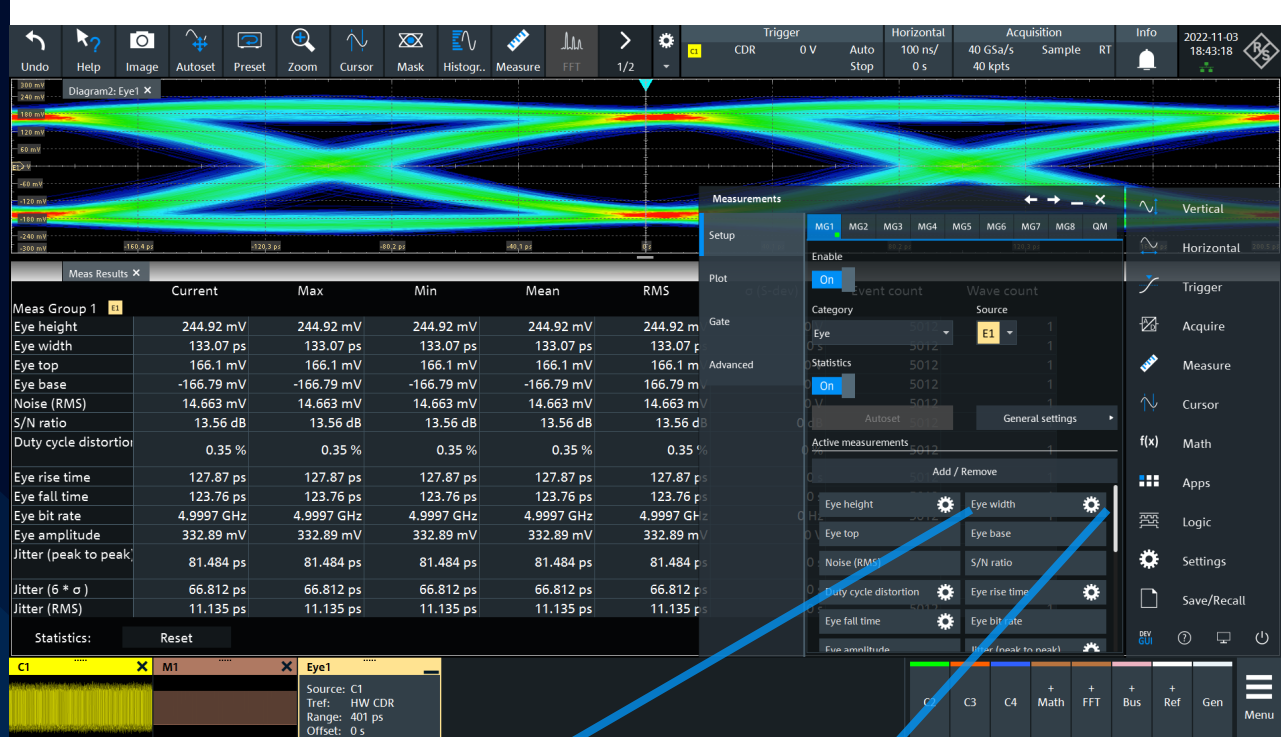
EYE STRIPE

- ▶ Couples mask violations with position in waveform
- ▶ Easy navigation between violations
- ▶ Coupled zoom to investigate details
- ▶ Time-correlation to other signals possible



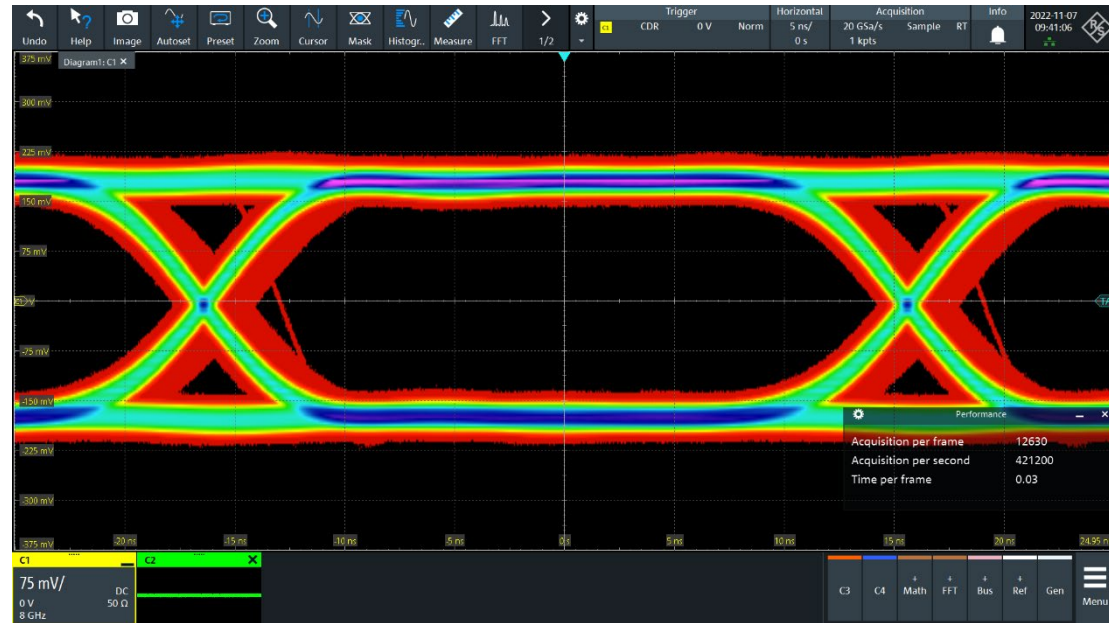
AUTOMATED EYE MEASUREMENTS

- ▶ 18 automated measurements
- ▶ Configure detailed measurement parameters



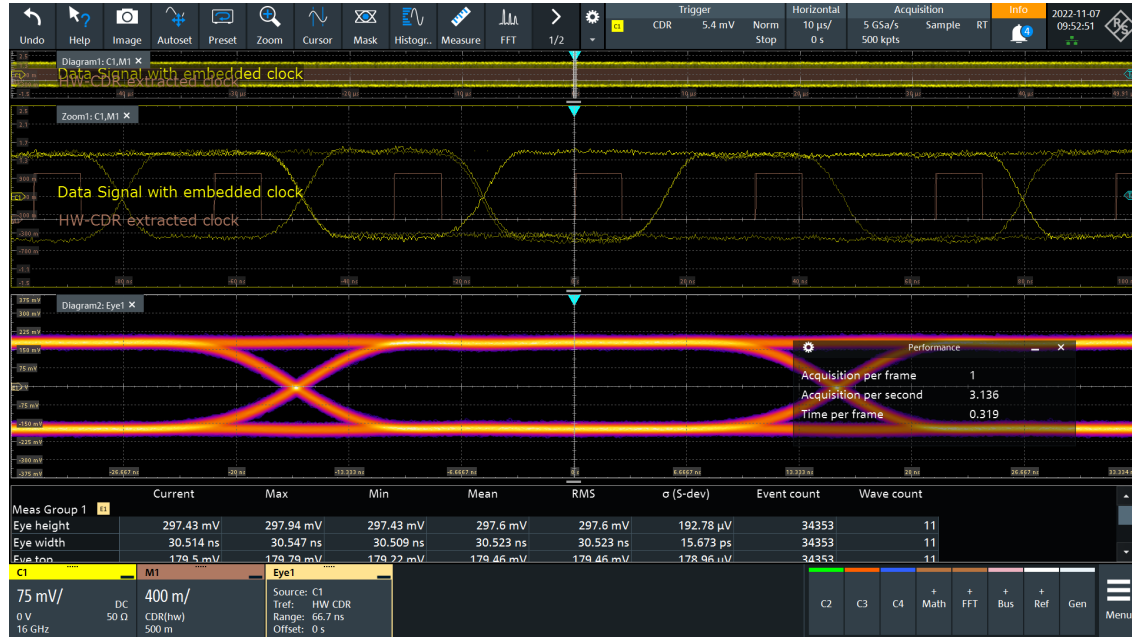
PERFORMANCE LIVE EYE

- ▶ Fastest: >420,000 UI/s
(20 GSa/s mode, RT, 1 kpts, dot)
- ▶ USB Demo (5 Gbps): ~200,000 UI/s
(40 GSa/s mode, IT)
- ▶ Minor impact of Analysis tools:
 - Mask test
 - Histogram
 - Automated Eye measurement



PERFORMANCE ADVANCED EYE

- ▶ Fastest: ~10,000 UI/s
- ▶ Further acceleration is planned
- ▶ Minor impact of Analysis tools:
 - Mask test
 - Histogram
 - Automated Eye measurement



COMPLIANCE TEST

The screenshot displays the R&S ScopeSuite software interface for a compliance test. The main window is titled "R&S ScopeSuite" and shows a session ID of "1.1_20240319_100950". The interface is divided into several sections:

- Top Bar:** Contains various utility icons (Undo, Redo, Recall, Save, Image, Zoom, Cursor, Mask, Measure, Annotate, FFT, Zone, Delete, Demo) and system information (Trigger: 880 mV, Width: > 500 μ s, Norm: Stop, Horizontal: 6.09 μ s/500 μ s, 10 GSa/s, 609 kpts, Acquisition: Sample, Hist 1, RT, Info, 2024-03-19 10:18:24).
- Left Panel:** Shows a tree view of test requirements:
 - All
 - Data Lane LP-TX Signaling Requirements (Group 1)
 - Clock Lane LP-TX Signaling Requirements (Group 2)
 - Data Lane HS-TX Signaling Requirements (Group 3)** (Selected)
 - Clock Lane HS-TX Signaling Requirements (Group 4)
 - HS Clock-To-Data Lane Timing Requirements (Group)
- Right Panel:** Displays test results in a table:

Test	Run	Result	Detail
1.1 HS Data Lane HS-TX Signaling Requirements	1	✓	27/27
- Bottom Panel:** Shows test status and configuration for three channels:
 - C1:** 250 mV/, 0 V DC-50 Ω , 3 GHz RTZD30
 - C2:** 165 mV/, 0 V DC-50 Ω , 3 GHz RTZD30
 - C4:** 165 mV/, 0 V DC-50 Ω , 3 GHz RTZD30

The background oscilloscope shows three waveforms: a yellow waveform (Differential Clock: C1), a green waveform (Dp: C2), and a blue waveform (Dn: C4). The test status at the bottom indicates "Test Data Lane HS-TX Signaling Requirements (Group 3) finished."

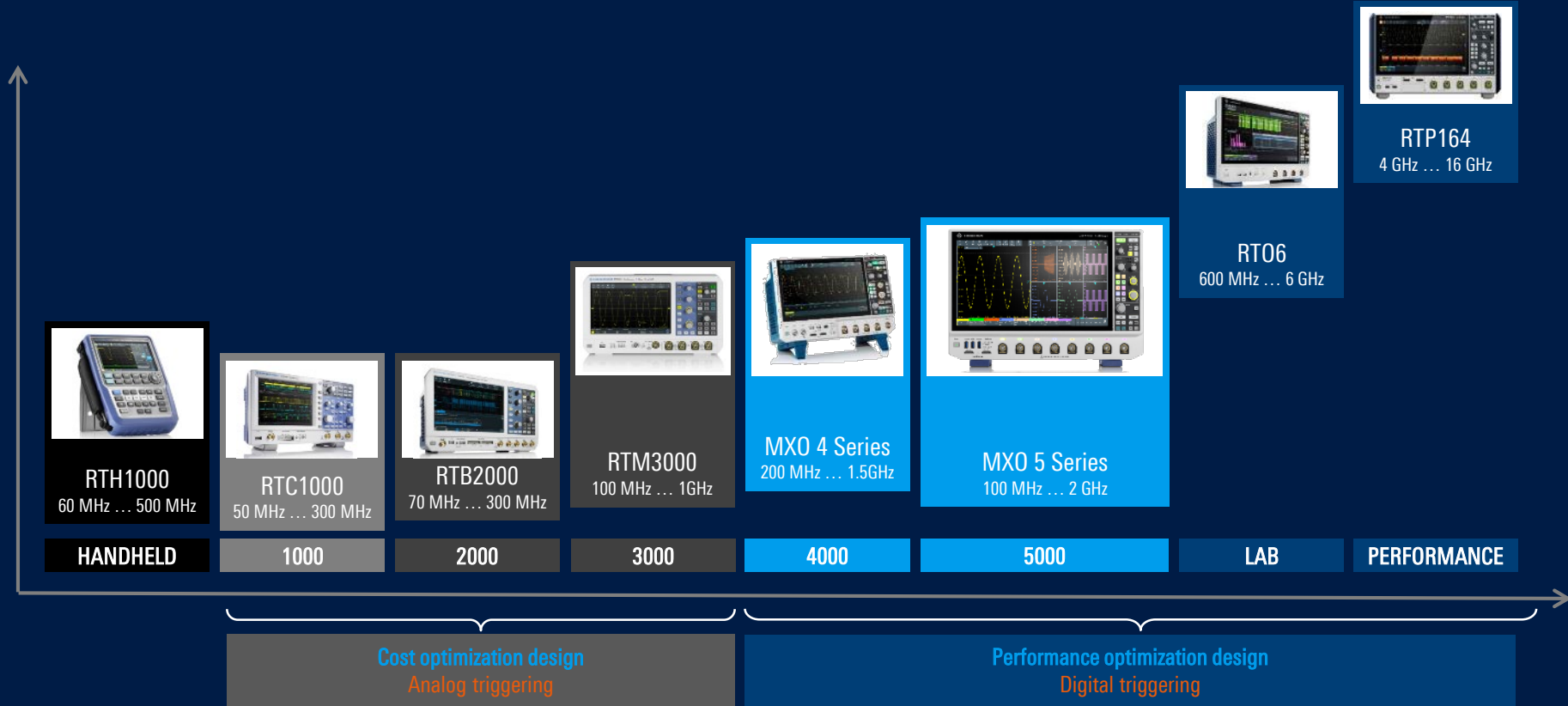
ADVANCED EYE ANALYSIS



DECODE



R&S OSCILLOSCOPE PORTFOLIO



Q & A